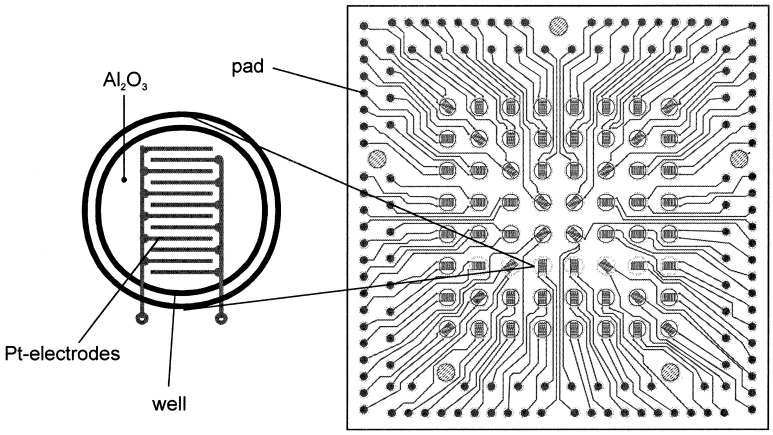
JOURNAL OF combinatorial CHEMISTRY

Article

Design Strategies for Multielectrode Arrays Applicable for High-Throughput Impedance Spectroscopy on Novel Gas Sensor Materials

U. Simon, D. Sanders, J. Jockel, C. Heppel, and T. Brinz

J. Comb. Chem., **2002**, 4 (5), 511-515• DOI: 10.1021/cc020025p • Publication Date (Web): 03 August 2002



More About This Article

Additional resources and features associated with this article are available within the HTML version:

- Supporting Information
- Links to the 6 articles that cite this article, as of the time of this article download
- Access to high resolution figures
- Links to articles and content related to this article
- Copyright permission to reproduce figures and/or text from this article

View the Full Text HTML

Journal of Combinatorial Chemistry is published by the American Chemical Society.
1155 Sixteenth Street N.W., Washington, DC 20036

Design Strategies for Multielectrode Arrays Applicable for High-Throughput Impedance Spectroscopy on Novel Gas Sensor Materials

U. Simon,*,† D. Sanders,† J. Jockel,† C. Heppel,‡ and T. Brinz‡

RWTH Aachen, Institut für Anorganische Chemie, D-52056 Aachen, Germany, and Robert Bosch GmbH, 70839 Gerlingen, Germany

Received April 3, 2002

This paper reports the first design and fabrication of a 64 multielectrode array for high-throughput impedance spectroscopy. The purpose of this work is the development of a measurement system for the discovery and improvement of sensor materials using combinatorial methods. An array of interdigital capacitors (IDC) screen-printed onto a high-temperature-resistant Al_2O_3 substrate is determined to be the optimal test plate. The electrode layout, and therefore also the idle capacity, is determined by specific requirements. Calculation of the idle capacity of the IDC as a function of the electrode width and distance allows adjustment and thus optimization of the array. Parasitic effects caused by the leads and contacts are compensated by a software-aided calibration. Apart from the use of the substrates for discovery of new sensor materials, the presented electrode array is also suitable for electrocatalytic applications as well as impedance spectroscopic studies of semiconductors and dielectrics.

Introduction

Sensor technology is one of the most important key technologies of the future with a constantly increasing number of applications, both in the industrial and in the private sectors. More and more gas sensors are used for the control of technical processes, in environmental monitoring, health care, and in automobiles. The development of fast and sensitive gas sensors with small cross sensitivity is therefore the subject of intensive research.

The main focus of traditional research on sensor materials is usually the optimization and modification of already known materials, although there may be a lot of new materials with better properties. Thus, it is definite that the demand for new materials for future sensor applications cannot be satisfied using conventional research methods, such as fabrication and sequential characterization of single sensors.

The discovery of new materials and new material combinations with improved properties is the subject of combinatorial materials research. For sensor technology, this means that using high-throughput methods will lead to totally new types of applicable materials and also to the optimization of existing materials in a wide parameter range. The premise for the development of new sensor materials is that both ion- and electron-conducting materials can be studied and that it is possible to examine further structure properties such as grain boundary conductance, interfacial polarization, and polarization of the electrodes.

This requires the use of complex impedance spectroscopy (IS) over a broad frequency range of $10-10^7$ Hz at temperatures from 293 to 1000 K. It is essential that the electrode arrays fulfill these requirements to be suitable for the intended application.

This paper will present the novel development of a 64 electrode array for high-temperature applications. The electrode arrays have been designed in such a way that both synthesis and measurement can be done directly on the plate using well-established methods employed in the fabrication of catalysts.[3,4]

Selection of the Material and Setup of the Multielectrode Array

The following points have been crucial for the selection of the substrate material: long-term stability against mechanical stress and thermal treatment, chemical resistance to the sample material, and a high electrical resistance. Therefore, Al_2O_3 was selected as the most suitable material.

Contrary to earlier work,[5−10] which describes the measurement of potentials and dc resistance, now not only the resistance but also the capacitive properties of the new materials can be determined. Therefore, an electrode layout formed as interdigital capacitors (IDC) is used. For the design of its structure width, the electrical properties and the shape of the sample on top of the capacitors have to be taken into consideration.

The platinum IDC is screen-printed onto an Al_2O_3 green tape with a structure width of 110 μm. This green tape is covered with a second green tape that has had holes punched at the appropriate positions to form the wells around the IDCs. They are laminated together and sintered for 2 days at 1350 °C. Hence, a pit is obtained for every IDC, which is termed "well". Each well has a diameter of 5 mm and a

* To whom correspondence should be addressed. Phone: +49-241-8094644. Fax: ++49-241-80 99003. E-mail: ulrich.simon@ac.rwth-aachen.de

† Institut für Anorganische Chemie.

‡ Robert Bosch GmbH.

10.1021/cc020025p CCC: $22.00
Published on Web 08/03/2002

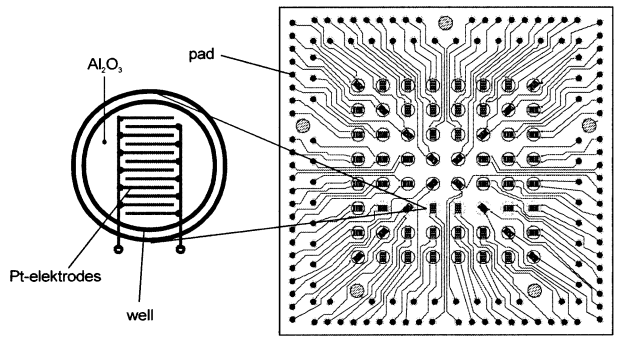


Figure 1. Layout of the multielectrode array.

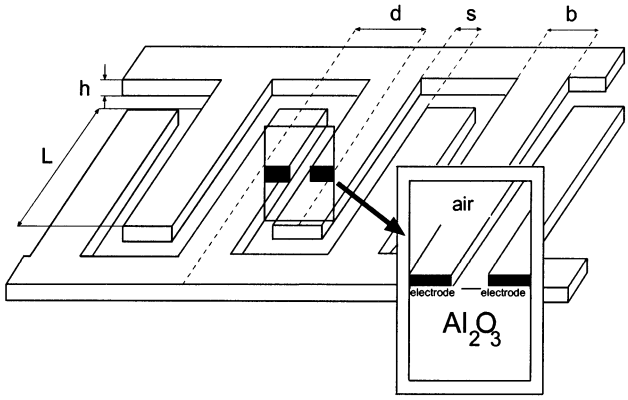


Figure 2. IDC structure with a unit cell.

maximum square contact area of 8 mm^2. To simplify the contact to the IDCs, a conductor path for each IDC leads to the area outside the array. Figure 1 shows the top view of the square substrate with a side length of 105 mm. The IDCs are arranged in an 8 × 8 array in the middle of the substrate. Connected to each IDC is the conductor path that leads to the contact pads on the outside of the array. Numbers according to the *xy* position are assigned to the IDCs.

Definition of the Layout Parameters

To allow the automatic dispensation of samples, the IDC contacts are positioned at the base of the well. The samples can be applied directly to the electrode structure, whereas the maximum height of the sample layer is determined by the depth of the well. So the ideal structure width of the IDC is predicted by the permittivity of the substrate material as well as by the maximum height of the sample layer. Figure 2 shows the schematic structure of the IDC.

Earlier investigations[11,12] have shown that the electrical field of the electrodes will decay within the sample layer if the height of the layer equals the distance between the electrodes. The height of the sample layer is 100−240 μm depending on the synthesis and sintering method. As an average of these values, a distance of $s = 170$ μm between the electrodes was chosen. On the basis of these layout parameters, the other structure parameters must be set in such a way that it is possible to measure high sample resistance and small changes in permittivity. Another consideration is that because of the roughness of the substrate, the grain size of the platinum paste, and the contraction during the sinter process, the substrate preparation has limited accuracy, leading to variations in the width and the distance between the electrodes. These variations should have the smallest possible effect on the distribution of the capacities of the IDC. Therefore, the width of the electrodes and consequently the number of electrodes have to be optimized by estimation of the capacity, considering the structure properties such as distance of the electrode, size of the well, and substrate permittivity.

The IDC consists of N fingers with length L, width b, distance s, and the height h. To compute the idle capacity of the empty IDC, the whole structure is approximated by an $(N - 1)$ times repetition of a unit cell. This is only possible if we neglect the influence of the boundaries, which is caused by large N ($N > 100$) or a large L/b or L/s ratio. The IDC described in this work has N as 12 and L equal to 2.1 mm. If the length depending capacity C'_{cell} of a unit cell is known, the capacity of the IDC is[11,12]

$$C_{\text{ges}} = C'_{\text{cell}}(N - 1)L \tag{1}$$

If the height of the electrode is neglected and if it is assumed that the thickness of the substrate is much larger than the electrode width b and the electrode distance s, the length-depending idle capacity C'_{cell} of the unit cell can be calculated using conformal mapping:[11,12]

$$C'_{0\text{cell}} = \frac{\epsilon_{\text{vacuum}} + \epsilon_{\text{substrate}}}{2} \frac{K(k)}{K(k')} \tag{2}$$

with

$$K(z) = \int_0^{\pi/2} \frac{\mathrm{d}x}{\sqrt{1 - z^2 \sin^2(x)}}$$

$$k' = \sqrt{1 - k^2}$$

$$k = \sin\left(\frac{\pi}{2} \frac{1}{q + 1}\right)$$

$$q = \frac{s}{b}$$

The analytical result for the capacity C'_{cell} of the unit cell only depends on the distance-to-width ratio of the electrodes. For comparison, the normalized IDC idle capacitance $C_{0\text{base}}$, based on an electrode area of 1 mm^2, is calculated from the cell capacitance as follows, taking the electrode width into consideration.

$$C_{0\text{base}} = C'_{0\text{cell}} \frac{1\ \text{mm}^2}{b(1 + q)} \tag{3}$$

The idle capacity of the IDC with an area of 7 mm^2 can be calculated from $C_{0\text{base}}$.

To demonstrate, Figure 3 shows the influence of the electrode width b and the electrode distance s on the dependency of the IDC idle capacity on the structural variation. It shows that the smaller the electrode width b and the smaller the layout parameter is, the bigger the variation of the idle capacity.

So an increasing q leads to a decrease in the error caused by the structural differences of the IDC. Assuming a constant electrode distance of $s = 170$ μm, the average error is

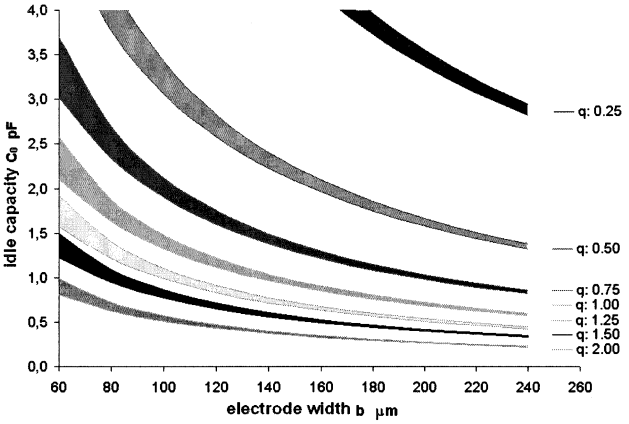


Figure 3. Analytically determined idle capacity C_0 of an empty IDC. The area is set to 7 mm^2. The idle capacity C_0 is shown as a function of the electrode width b. Each graph has a different layout parameter $q = s/b$. The width of the graph shows the distribution of the idle capacity C_0 as the electrode varies by 10 μm.

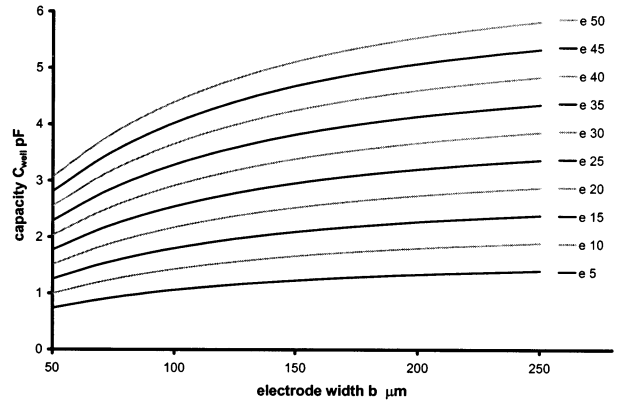


Figure 4. Analytical solution of the IDC capacity C_{well} as a function of the electrode width assuming a permittivity of $\epsilon_{substrate} = 8.3$ and with varying permittivities of the sample material with a fixed electrode distance of $s = 170$ μm.

sufficiently small if the electrode width is >100 μm. Figure 4 shows the dependency of the capacity on the electrode width when the electrode distance is set to 170 μm. The parameter of the different graphs is the permittivity ($\epsilon = 5-50$) of the sample material coated onto the IDC.

So an increase of the electrode width leads to a better measurement accuracy, i.e., a better resolution. The electrode width has to be larger than 100 μm to achieve suitable accuracy for measuring capacities.

Taking all mentioned parameters into account, the optimal base electrode width for our application is $b = 110$ μm.

Influence of the Conductor Pathway

The conductor path to each IDC differs in length and distance because of the compact setup of the IDC and the central positioning of the 64 wells on the substrate. The conductor path is parallel to the IDC, so both capacities are added. Hence, we get a broad distribution of the measured capacities including large differences from the calculated value. This problem is demonstrated in Figure 5, which shows the measured capacities C_{0exp} of the IDC on the substrate.

The capacity of the conductor path is approximated by the capacity of a pair of leads. The capacity of a pair of

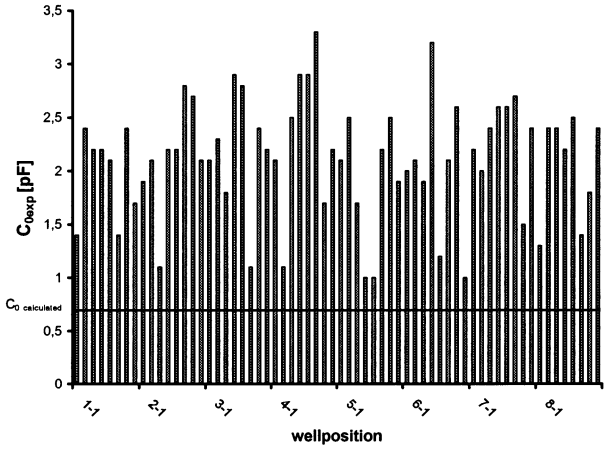


Figure 5. Measured capacities of the IDC (C_{0exp}) of all wells compared with the calculated idle capacity of the IDC without the conductor paths.

Table 1. Comparison of the Calculated and Measured Total Capacities

well	IDC capacity according to eqs 2 and 3 (pF)	lead capacity according to eq 4 (pF)	calculated total capacity (pF)	measured total capacity (pF)
4-6	0.7 ± 0.2	3.2 ± 0.8	3.9 ± 1	3.3
5-5	0.7 ± 0.2		0.7 ± 0.2	1.0

leads with radius r, length l within a distance of a, and a permittivity of ϵ is[13]

$$C_{lead} = \frac{\pi \epsilon l}{\ln\left(\frac{a}{r}\right)} \tag{4}$$

ϵ is the effective permittivity of the space between the leads, and the radius r is set to half of the width of the conductor path.

Owing to the complex pathways of the conductor leads, the length and especially the distance between the conductor paths cannot be easily determined. For this reason, only two well positions with the most differing pathways are examined. The first is position 4-6. Its conductor pathways are parallel and have a length of ca. 30 mm with a distance of 750 μm in between. Approximated with the capacity of a pair of leads, we get $C_{path} = 3.2 \pm 0.8$ pF. The other position is 5-5. The conductor pathways are adjacent to each other, so the capacity is negligible. Table 1 shows a comparison of the calculated capacities with the measured values.

Table 1 demonstrates that the variation of the experimentally measured values of the 64 IDC idle capacities is caused by the differences in the capacities of the conductor path.

Compensation of Parasitic Effects

Owing to the complex layout of the conductor leads and the necessary approximations, the electrical characteristics of each well cannot be calculated analytically. The parasitic effects therefore have to be determined by a compensation measurement. The circuit equivalent of the parasitic effects consists of a lead, contact resistance R_s, and lead inductance L_s in series as well as a stray capacitance C_0 and the

Chart 1

$$R_P = \frac{(R_M - R_S)[1 - G_0(R_M - R_S)] - G_0(X_M - \omega L_S)^2}{[1 - G_0(R_M - R_S) + \omega C_0(X_M - \omega L_S)]^2 + [G_0(X_M - \omega L_S) + \omega C_0(R_M - R_S)]^2} \quad (5)$$

$$X_P = \frac{(X_M - \omega L_S)[1 + \omega C_0(X_M - \omega L_S)] - \omega C_0(R_M - R_S)^2}{[1 - G_0(R_M - R_S) + \omega C_0(X_M - \omega L_S)]^2 + [G_0(X_M - \omega L_S) + \omega C_0(R_M - R_S)]^2} \quad (6)$$

$$G_P = \frac{(G_M - G_0)[1 - R_S(G_M - G_0)] - R_S(B_M - \omega C_0)^2}{[1 - R_S(G_M - G_0) + \omega L_S(B_M - \omega C_0)]^2 + [R_S(B_M - \omega C_0) + \omega L_S(G_M - G_0)]^2} \quad (7)$$

$$B_P = \frac{(B_M - \omega C_0)[1 + \omega L_S(B_M - \omega C_0)] - \omega L_S(G_M - G_0)^2}{[1 - R_S(G_M - G_0) + \omega L_S(B_M - \omega C_0)]^2 + [R_S(B_M - \omega C_0) + \omega L_S(G_M - G_0)]^2} \quad (8)$$

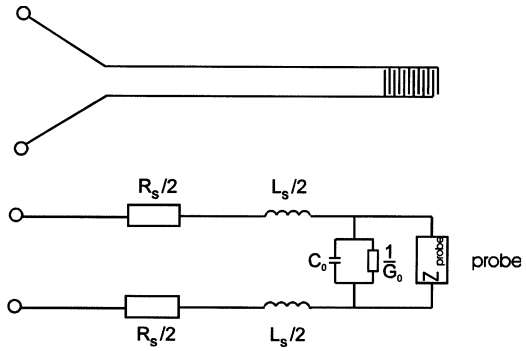


Figure 6. Interdigital capacitor with parallel leads and the corresponding equivalent circuit.

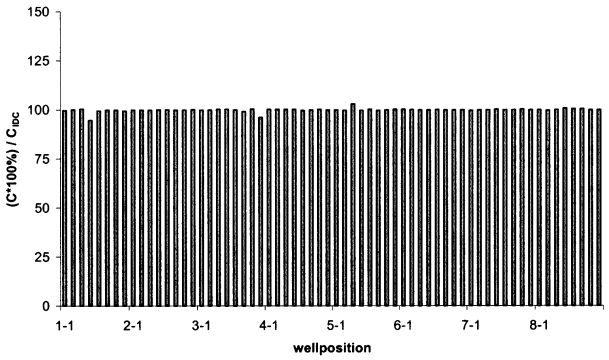


Figure 7. Adjusted capacities of the well positions, normalized to the calculated capacity of an IDK.

resistance of the isolating material between the leads $1/G_0$ parallel to the impedance of the probe. Knowing all parasitic factors in the whole frequency range, the impedance of the probe Z_{probe} can be calculated from the measured values Z_M using the method described in ref 15. Measurement errors caused by a lead impedance in series are determined by a measurement with shorted electrodes. Parasitic effects due to stray capacitance are measured with an isolating sample on the IDC.

When the equivalent circuit in Figure 6 is used, the impedance $Z_{probe} = R_P + jX_P$ and the admittance $Y_{probe} = G_P + jB_P$ of the sample can be calculated. The subscripts in the following equations denote the type of measurement. M signifies the measurement with sample, S the short measurement, and O the open measurement. According to Kirchhoff's law, eqs 5−8 are as shown in Chart 1.

Equations 5−8 are used in the measurement software to calculate the compensated values. The results of the compensation are shown in Figure 7. A comparison of Figure 5 to Figure 7 shows the adjusted capacities (normalized to the calculated capacity) of the well positions. The homogeneity of the capacities proves the applicability of the compensation of parasitic effects.

Conclusion

The 64 multielectode array presented in this paper enables electrical high-throughput studies of potential sensor materials. By adjustment of the electrode layout, complete impedance spectroscopic characterization can be performed. Parasitic effects, resulting from the compact arrangement of the electrodes, can be eliminated by a software-based offset adjustment. This development will be a key feature in the discovery of new materials for a broad range of applications in chemical sensing, catalysis, and miroelectronics.

Acknowledgment. Financial support is from bmb+f (Bundesministerium für Bildung und Forschung) (Grant FKZ03C0305).

References and Notes

(1) Gas-Sensing Materials. *MRS Bull.* **1999**, *24*, 6.
(2) Liu, Y.; Cong, P.; Doolen, R. D.; Turner, W. W.; Weinberg, W. H. *Catal. Today* **2000**, *61*, 87.
(3) Maier, W. F. *Angew. Chem.* **1999**, *111* (9), 1294−1296.
(4) Klein, J.; Lehmann, C. W.; Schmidt, H.-W.; Maier, W. F. *Angew. Chem.* **1998**, *110*, 3557−3561; *Angew. Chem., Int. Ed.* **1998**, *37*, 3369−3372.
(5) Briceno, G.; Chang, H.; Sun, X.; Schulz, P. G.; Xiang, X. D. *Science* **1995**, *270*, 273.
(6) Xiang, X. D.; Sun, X.; Briceno, G.; Lou, Y.; Wang, K.; Chang, H.; Wallace-Freedman, W. G.; Chen, S.; Schulz, P. G. *Science* **1995**, *268*, 1738.
(7) Somov, S.; Reinhardt, G.; Guth, U.; Göpel, W. *Sens. Actuators, B* **1996**, *35*−*36*, 409.
(8) Albert, K. J.; Lewis, N. S.; Schauer, C. L.; Sotzing, G. A.; Stitzel, S. E.; Vaid, T. P.; Walt, D. R. *Chem. Rev.* **2000**, *100*, 2595.
(9) George, M.; Parak, W. J.; Gaub, H. E. *Sens. Actuators, B* **2000**, *69*, 266.
(10) Capone, S.; Siciliano, P.; Quaranta, F.; Rella, R.; Epifani, M.; Vasanelli, L. *Sens. Actuators, B* **2000**, *69*, 230.
(11) Scheibe, C.; Obermeier, E.; Maunz, W.; Plog, C. Design and realisation of a direct heatable gas sensor basis structure for temperatures up to 450 °C (in German); ITG-Fach-

bericht, 126; VDE-Verlag GmbH: Berlin, 1994 (ISBN 3-8007-1988-6).
(12) Scheibe, C.; Obermeier, E.; Maunz, W.; Plog, C. *Sens. Actuators, B* **1995**, *25*, 584.
(13) *Lexikon der Physik* (Lectures in Physics); Francke, H., Ed.; Franck'sche Verlagsbuchhandlung: Stuttgart, 1969.
(14) Operation Manual Agilent 4192A, Agilent Technologies, Kobe, Japan, 2000.
(15) Thomae, E. Ph.D. Thesis, University of Essen, Germany, 1990.

CC020025P